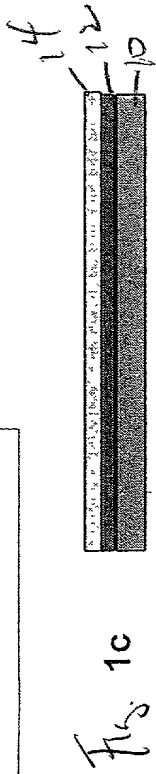


Reverse Neo Process

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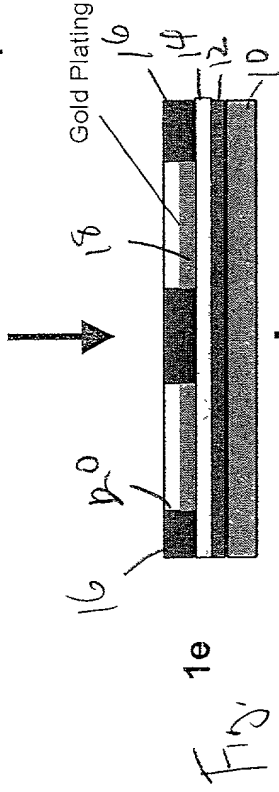
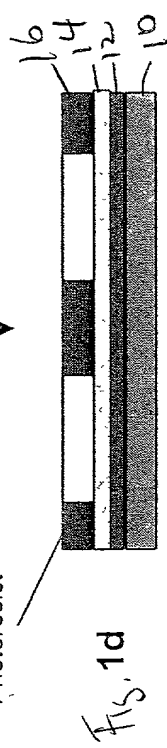
1c) Apply field metal

1d) Apply photoresist

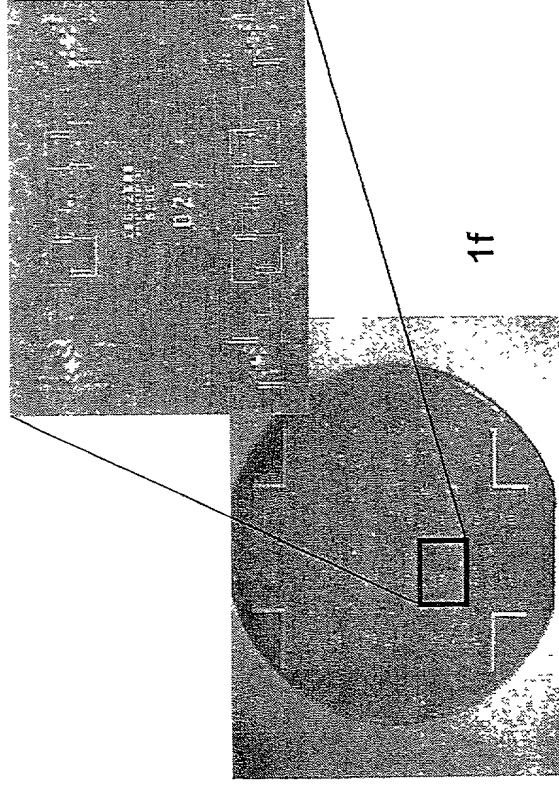
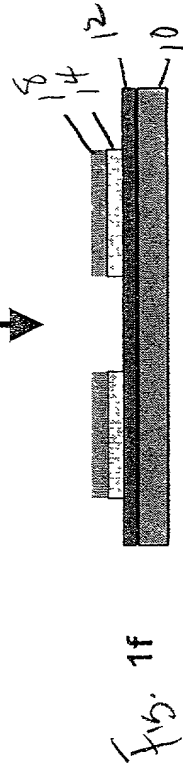
1e) Gold electroplate

1f) Strip photoresist & field metal etch

Photoresist



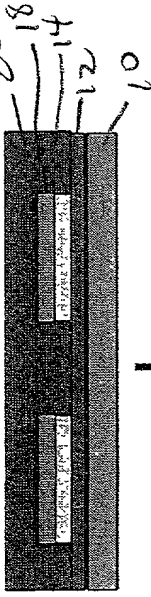
Gold Plating



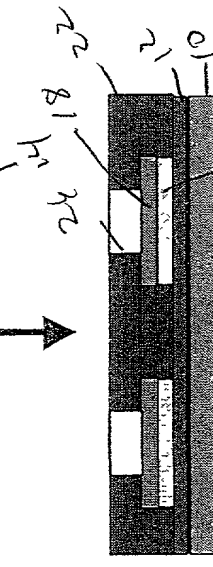
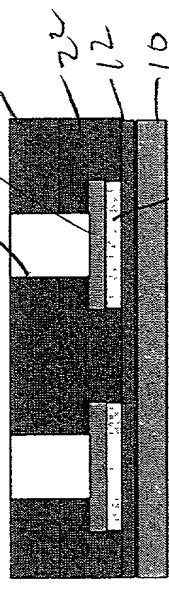
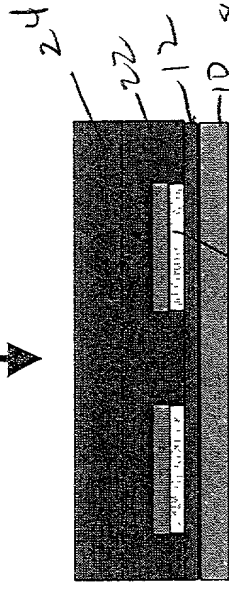
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Reverse Neo Process

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- 1g) Apply polyimide
- 1h) Apply photoresist
- 1i) Image & develop photoresist & polyimide
- 1j) Strip photoresist & cure polyimide



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Reverse Neo Process

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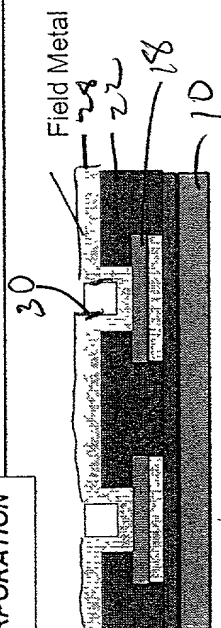


Fig. 1k



- 1k) Apply field metal
- 1l) Apply photoresist
- 1m) Image & develop photoresist. Gold electroplate
- 1n) Strip photoresist & field metal etch

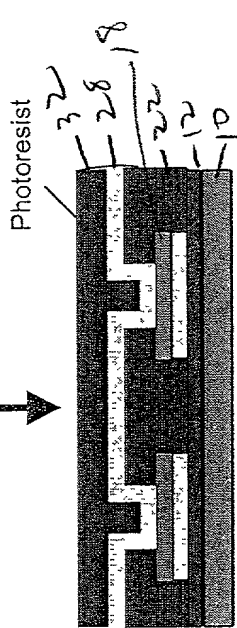


Fig. 1l

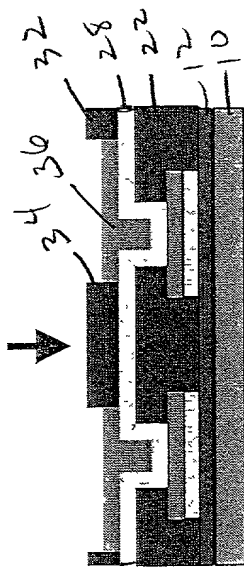


Fig. 1m

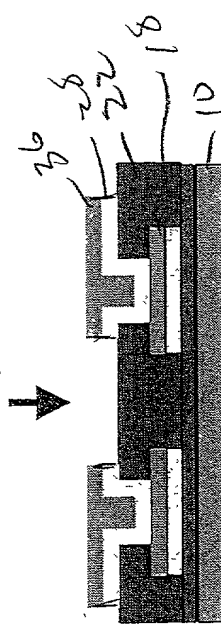


Fig. 1n

NOTE: For additional layers, steps 1g through 1n are repeated.

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Reverse Neo Process

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Solder Bumping Of Die

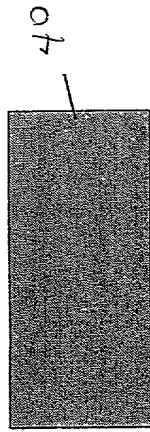


Fig. 2a

- 2a) Retrieve die
- 2b) Apply underbump metalurgy
- 2c) Apply solder bump

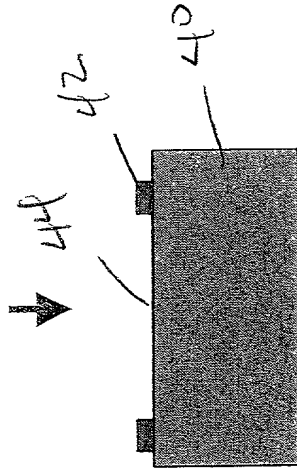


Fig. 2b

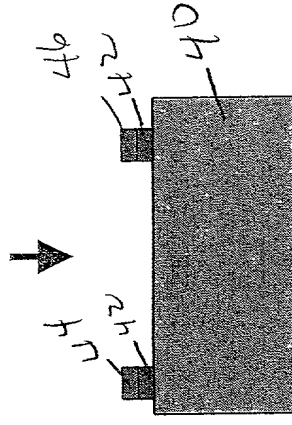
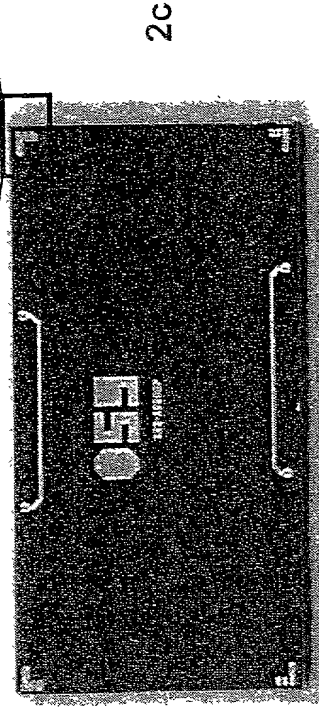
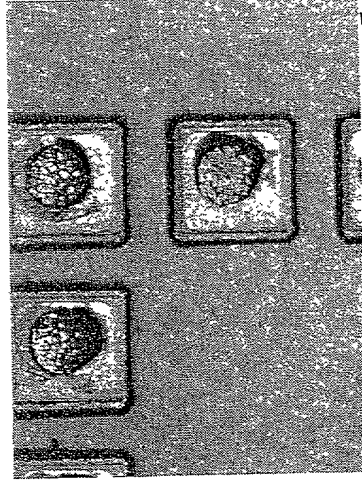


Fig. 2c

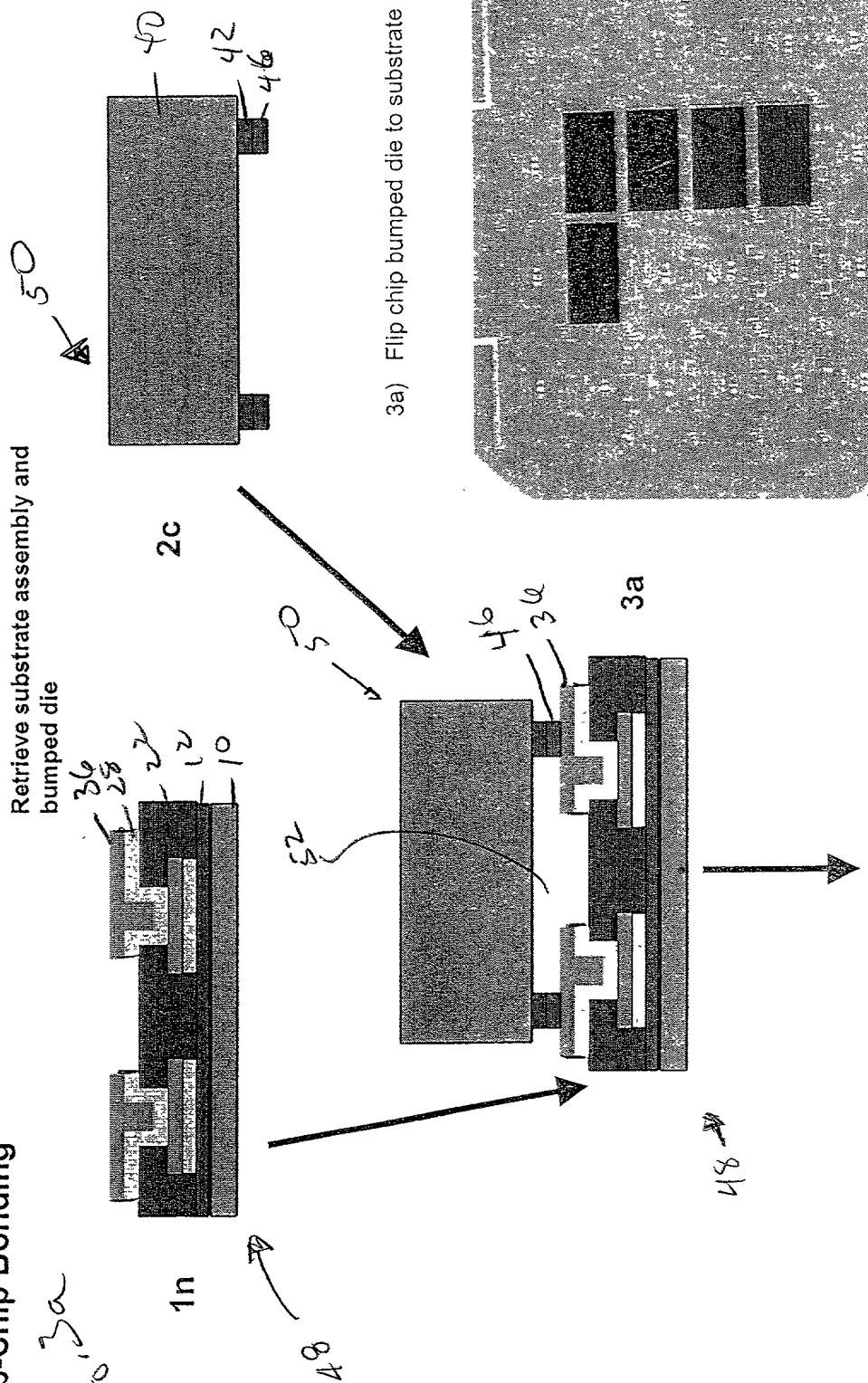


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Flip-Chip Bonding

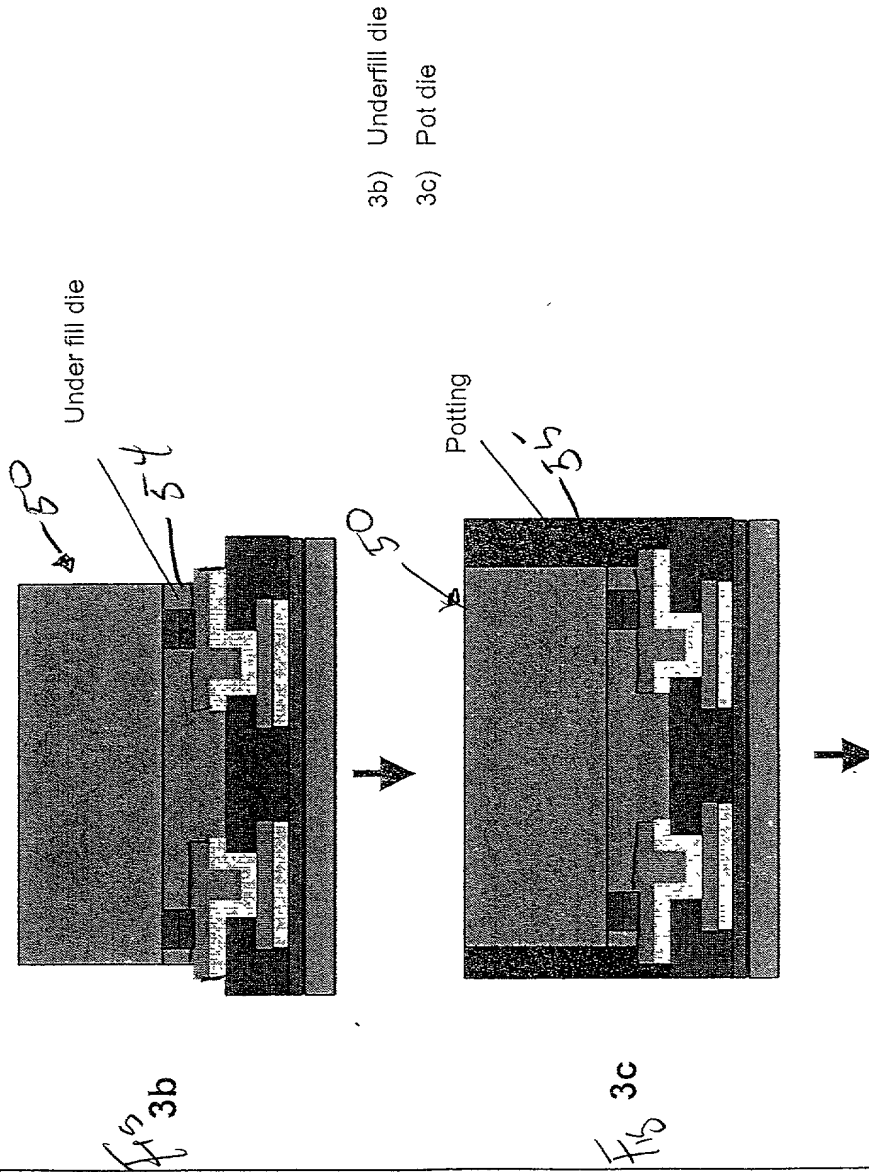
Fig. 3a



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FIGURE 3b Reverse Neo Process

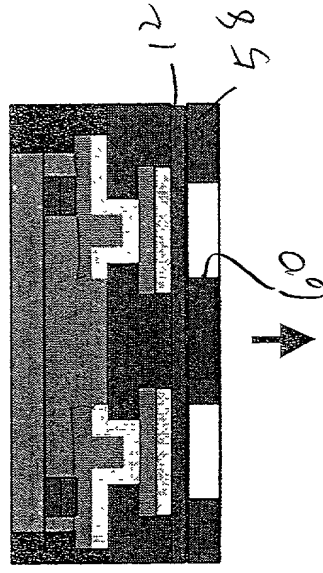
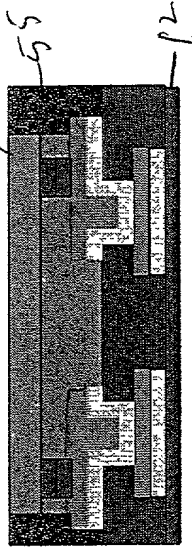
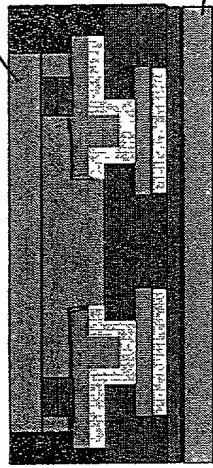
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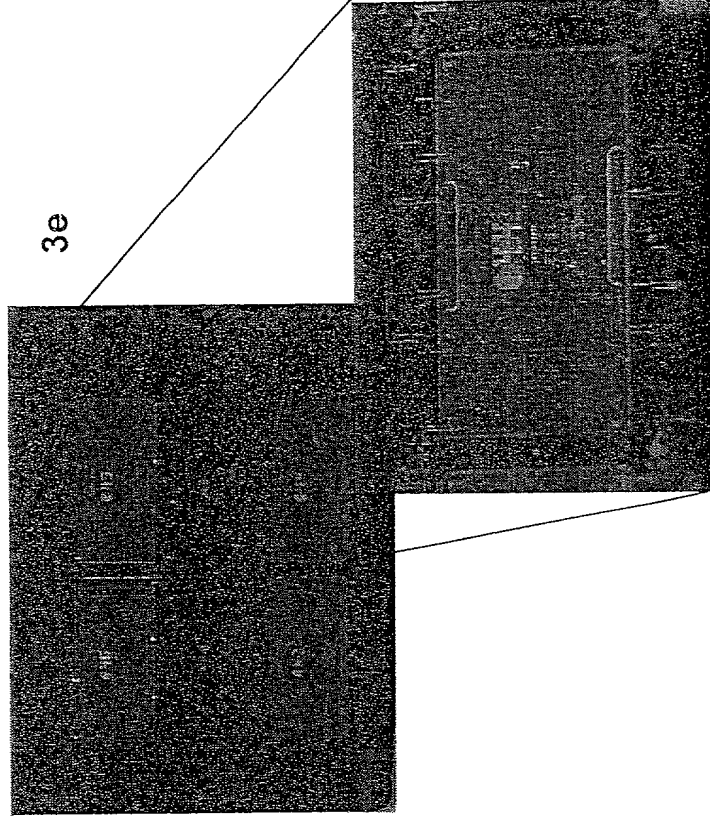
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Reverse Neo Process

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- 3d) Thin wafer
- 3e) Release wafer from aluminum substrate
- 3f) Mask wafer for test pad etch



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Reverse Neo Process

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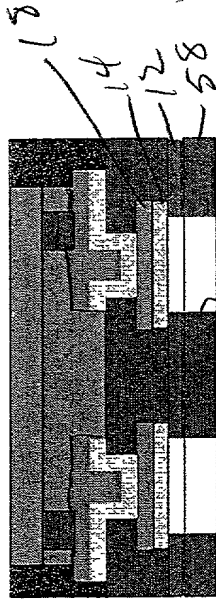


Fig 3g

- 3g) Etch polyimide to expose test pads
- 3h) Remove etch mask & test wafer
- 3i) Dice wafer

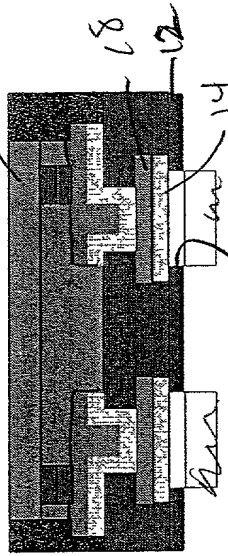


Fig 3h

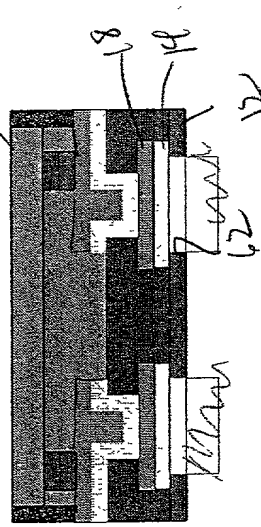
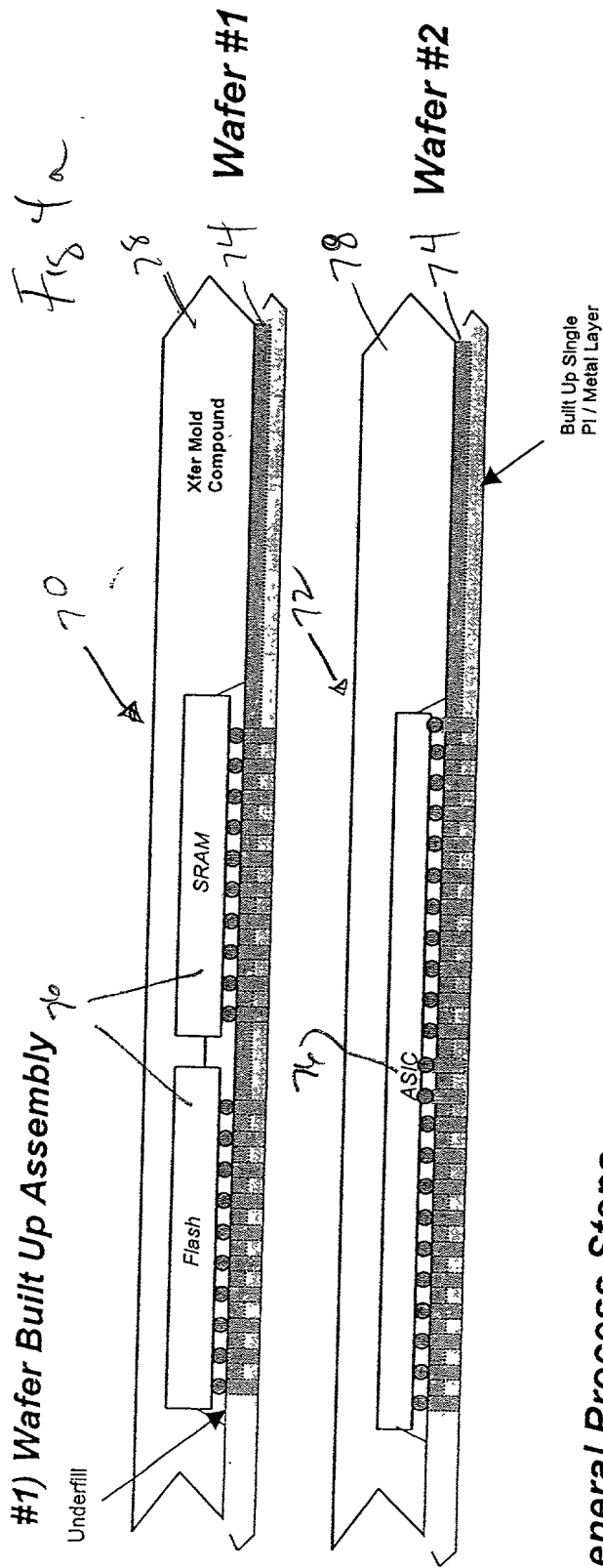


Fig 3i

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High Volume Reverse NEO Process



General Process Steps

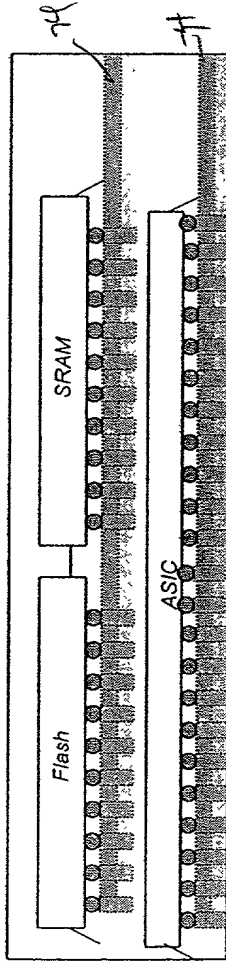
- 1) Screen Print Electrically Conductive Epoxy on Built-Up Laminate Substrates
- 2) Place Flip Chip Devices
- 3) Cure Epoxy
- 4) Underfill Devices
- 5) Xfer. Mold Devices

High Volume Reverse NEO Process

2) Stacked Wafer Strip Assembly

General Process Steps

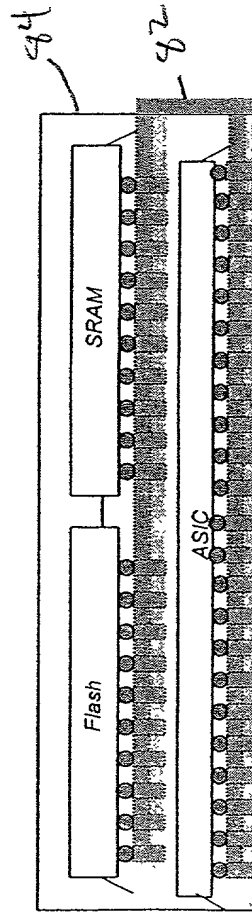
- 6) Release Carrier Film from Substrate (If Required)
- 7) Attach Memory and ASIC Wafers
- 8) Cut/Saw Wafers to Strips



3) Stacked Wafer Strip Assembly

General Process Steps

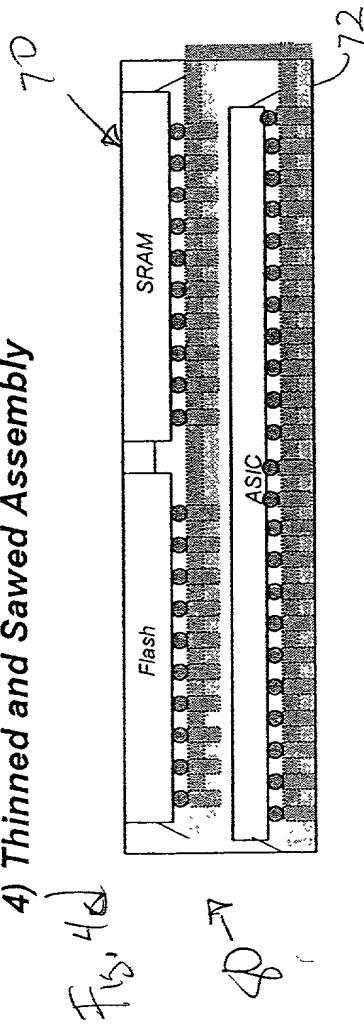
- 9) Interconnect or Bus Wafers by Metallizing Wafer Stacks



High Volume Reverse NEO Process

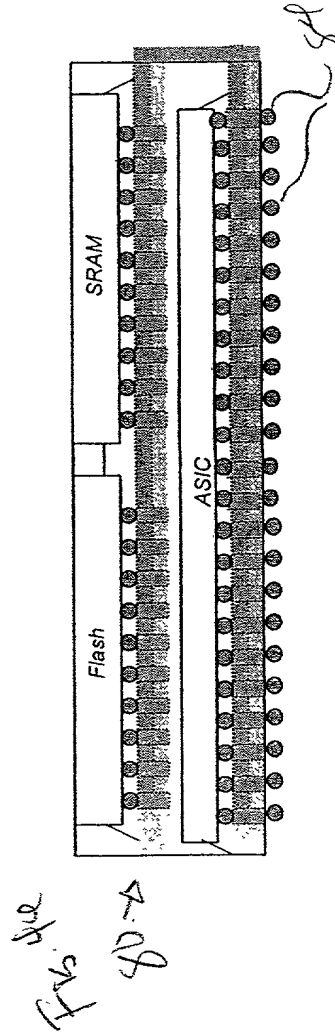
General Process Steps

4) Thinned and Sawed Assembly



10) Thin Stack Assembly

5) Thinned and Sawed Assembly



General Process Steps

- 11) Solder Bump Stack
- 12) Singulate (Saw) into Individual Stacks